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25M1/0323

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ART UNIT	PAPER NUMBER
	2

2511
DATE MAILED:

03/23/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined Responsive to communication filed on _____ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. Notice of References Cited by Examiner, PTO-892.
2. Notice re Patent Drawing, PTO-948.
3. Notice of Art Cited by Applicant, PTO-1449.
4. Notice of informal Patent Application, Form PTO-152.
5. Information on How to Effect Drawing Changes, PTO-1474.
6. _____

Part II SUMMARY OF ACTION

1. Claims 1-24 are pending in the application.

Of the above, claims _____ are withdrawn from consideration.

2. Claims _____ have been cancelled.

3. Claims _____ are allowed.

4. Claims 1-24 are rejected.

5. Claims _____ are objected to.

6. Claims _____ are subject to restriction or election requirement.

7. This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. Formal drawings are required in response to this Office action.

9. The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are acceptable. not acceptable (see explanation or Notice re Patent Drawing, PTO-948).

10. The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been approved by the examiner. disapproved by the examiner (see explanation).

11. The proposed drawing correction, filed on _____, has been approved. disapproved (see explanation).

12. Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has been received not been received been filed in parent application, serial no. _____; filed on _____.

13. Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. Other

EXAMINER'S ACTION

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Claims 8, 11-14 and 22-24 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 8, line 6, "said first and second banks" has no antecedent basis.

In claim 14, lines 11, 12 and 17, "sense amplifiers", it is not clear if these are the same as "slave amplifiers".

In claim 22, line 12 and claim 24, line 2, "data" it is not clear if this is the same data as in claim 22, line 10.

In claim 23, line 2, "other cells", it is not clear if these are the same as cells in claim 22, line 13.

The disclosure is objected to because of the following informalities: In claim 9, line 3, claim 11, lines 4, 7, 10, 13, "the" should be deleted. Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 7-10 are rejected under 35 U.S.C. § 102(e) as being anticipated by Iwase.

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Iwase in figures 2 discloses a memory comprising an array of cells (11), row address circuitry (12) for access to cells, sense amplifiers (13) coupled to bit lines, latches (slave amplifiers) (14) coupled to amplifiers, column decoder (15, 16) coupled to latches and control circuitry. The control circuitry comprises mode control circuitry (clock generator, not shown), and multiplexed (19) coupled to the latches, where different data are read to the latch through the amplifier and are supplied to output (18).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shikata.

Shikata in figures 1 and 2 discloses a memory comprising; DRAM cell array (5), row decoder (3) for accessing the cells, read/write amplifier (6), first and second sense amplifier, latch circuitry (8, 22) for storing data for exchange with amplifier.

Claims 1-7, 9, 10 and 15-24 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kanabara.

Kanabara in figures 1, 8, 10, 12 and 19 discloses a memory device and method of reading and writing comprising; a DRAM array (1) arranged in rows and columns, row decoder (3) coupled to word lines, amplifier circuit (9, 10) coupled to the bit lines, column decoder (6,8) coupled to data, first and second latch circuitry

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(7) coupled to the amplifier and column decoder, control circuitry (3) for alternately latching data between latches and sense amplifier. While data in a portion of latch is exchanged (read/write) with amplifier or decoder, a second data can be exchanged (read/write) in another portion of the latch circuit which is selected by decoder (see abstract and col. 13, lines 1-11 and fig. 19).

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 8, 11 and 12 are rejected under 35 U.S.C. § 103 as being unpatentable over Kanabara in view of Shikata.

Kanabara as applied in prior rejection discloses every claimed subject matter except details of controller (3). Shikata as applied in prior rejection in figures 3 and 4 teaches the use of multiplexers for producing timing signals for controlling

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different blocks. Therefore it would have been obvious to one of ordinary skill in the art to use a multiplexer in controller (3) of Kanabara for producing timing signals.

Claims 13 and 14 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.

The prior art does not disclose reading a section of a cell array selected by a row decoder into a slave sense amps through master sense amps and shifting and writing the same data into another section of the array selected by the decoder through the master sense amplifier.

Any inquiry concerning this communication should be directed to A. Zarabian at telephone number (703) 308-4905.

Zarabian/tj
March 20, 1995


A. Zarabian
Exr. 25/11